

IN THE CLAIMS

1-9 (Previously Canceled)

10. (Currently Amended) A transistor formed in a semiconductor substrate, the substrate having a first conductivity type and a surface, the transistor comprising:

ca a collector region having an impurity therein which promotes one of either holes or electrons as a majority carrier, the collector region extending downward from the surface of the substrate, wherein the first conductivity type of the substrate promotes the other of either holes or electrons as a majority carrier;

a base region having an impurity therein which promotes the other type of carrier, the base region having a surface area and extending downward from the surface of the substrate into contact with a portion of the collector region;

an emitter on top of the base region and having a surface area smaller than the surface area of the base region; and

an implant area of the collector region vertically adjacent to the base region having an increased collector doping of an implanted impurity, the implant area having an effective top surface area greater than the surface area of the emitter and less than the surface area of the base region.

11. (Previously Added) The transistor of claim 10, wherein the transistor is an NPN transistor and the implant impurity in the implant area of the collector region is phosphorous.

12. (Previously Added) The transistor of claim 10, wherein the transistor is a PNP transistor and the implant impurity in the implant area of the collector is boron.

13. (Currently Amended) A transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

a base region having an impurity therein which promotes the first majority carrier, the base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region on the base region, the emitter region having a surface area smaller than a surface area of the base region; and

an implant region interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective top surface area greater than the surface area of the emitter region and less than the area of the base region contiguous to the collector region.

14. (Previously Added) The transistor of claim 13, wherein the transistor is an NPN transistor and the implant impurity in the implant region is phosphorous.

15. (Previously Added) The transistor of claim 13, wherein the transistor is a PNP transistor and the implant impurity in the implant region is boron.

16. (Currently Amended) The transistor of claim 13, wherein the effective top surface area of the implant region minimizes carrier injection from the emitter region to the collector region outside of the implant region at high current operation of the transistor.

17. (Currently Amended) A transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

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a base region having an impurity therein which promotes the first majority carrier, the base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region on the base region, the emitter region having a surface area smaller than a surface area of the base region;

a first implant region interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective top surface area greater than the surface area of the emitter region and less than the area of the base region contiguous to the collector region; and

a second implant region formed in the collector region.

18. (Previously Added) The transistor of claim 17, wherein the second implant region is formed at about the same level from the surface of the substrate as the first implant.

19. (Previously Added) The transistor of claim 17, wherein the collector region includes a plug extending from the surface of the substrate, the plug being separate from the base region.

20. (Previously Added) The transistor of claim 19, wherein the second implant region is formed in the plug at about the same level from the surface of the substrate as the first implant region.

21. (Previously Added) The transistor of claim 17, wherein the transistor is an NPN transistor and the implant impurity in the first and second implant regions is phosphorous.

22. (Previously Added) The transistor of claim 17, wherein the transistor is a PNP transistor and the implant impurity in the first and second implant regions is boron.

23. (Currently Amended) The transistor of claim 17, wherein the effective top surface area of the first implant region minimizes carrier injection from the emitter region to the collector region outside the first implant region at high current operation of the transistor.

24. (Previously Added) The transistor of claim 17, wherein the second implant region has a surface area greater than the area of an opening through which the second implant region is formed.

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25. (Currently Amended) A transistor, comprising:  
an emitter having an emitter surface area;  
a base having a base surface area;  
a collector in contact with the base; and  
an implant region intermediate the base and the collector, the implant region having an implant top surface area greater than the emitter surface area and less than the base surface area.

26. (Currently Amended) The transistor of claim 25 wherein the collector has a collector surface area, and the implant region top surface area is less than the collector surface area.

27. (Previously Added) The transistor of claim 26, wherein the base surface area is less than the collector surface area.

28. (Currently Amended) The transistor of claim 26, wherein the base surface area and the implant region top surface area where both contact the collector have a combined area greater than the emitter surface area.

29. (Previously Added) The transistor of claim 26, wherein the base directly contacts both the collector and the implant region.

30. (Currently Amended) A transistor device formed in a semiconductor substrate comprising:

a diffused n well collector region having an impurity of a first conductivity type, the collector region extending downwardly from a surface of the substrate, the substrate being generally doped with an impurity of a second conductivity type;

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cont a base region having an impurity of the second conductivity type doped at a generally constant doping level across a surface thereof, the base region extending downwardly from the surface of the substrate into contact with a portion of the collector region;

an emitter having an impurity of the first conductivity type on top of the base region and having a surface area smaller than a surface area of the base region; and

~~an~~ a top area of the collector region vertically adjacent the base region having an increased collector doping of the first conductivity type, the top area of the collector region having an effective surface area in contact with the base region that is greater than the surface area of the emitter.

31. (Previously Added) The transistor device of claim 30, wherein the impurity of the first conductivity device is phosphorous.

32. (Currently Amended) The transistor device according to claim 30, wherein the effective top area surface area of the collector region is less than less than a non-increased doped area of the portion of the collector region in contact with the base region.

33. (Currently Amended) A transistor formed in a substrate, the substrate having a first conductivity type and a surface, the transistor comprising:

a collector region having a first impurity means for promoting one of either holes or electrons as a majority carrier, the collector region extending downward from the surface of the substrate, wherein the first conductivity type of the substrate promotes the other of either holes or electrons as a majority carrier;

a base region having a second impurity means for promoting the other type of carrier, the base region having a surface area and extending downward from the surface of the substrate into contact with a portion of the collector region;

an emitter region on top of the base region and having a surface area smaller than the surface area of the base region; and

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cont. an implant area of the collector region vertically adjacent to the base region having an increased collector doping of an implanted impurity, the implant area having an effective top surface area greater than the surface area of the emitter region and less than the surface area of the base region.

34. (Currently Amended) A transistor, comprising:

an emitter having an emitter surface area;

a base having a base surface area;

a collector in contact with the base;

a collector plug in the collector;

a first implant region intermediate the base and the collector, the first implant region having an implant top surface area greater than the emitter surface area and less than the base surface area; and

a second implant region in the collector plug.

35. (Previously Added) The transistor of claim 34, wherein the first implant region and the second implant region are positioned at a same depth.

36. (Previously Added) The transistor of claim 34, wherein the first implant region and the second implant region are simultaneously formed by an angled implant such that areas of the first implant region and the second implant region are greater than areas of the openings through which the first implant region and the second implant region are formed.

37. (Previously Added) The transistor of claim 34, wherein the first implant region and the second implant region are doped by a same source.

38. (Previously Added) A transistor, comprising:

an emitter having a periphery;

a base in contact with the emitter;

a collector in contact with the base; and

means for minimizing carrier injection from the periphery of the emitter region to the collector region at high current operation of the transistor.

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Concl. 39. (Previously Added) The transistor of claim 38, wherein means for minimizing carrier injection includes an implant region intermediate the base and the collector, the implant region having an implant surface area greater than a surface area of the emitter and less than a surface area of the base.

40. (Previously Added) A transistor, comprising:

an emitter;

a base in contact with the emitter;

a collector in contact with the base; and

means for minimizing base-collector capacitance and maximizing high current operation.

41. (Previously Added) The transistor of claim 40, wherein means for minimizing base-collector capacitance and maximizing high current operation includes an implant region intermediate the base and the collector, the implant region having an implant surface area greater than a surface area of the emitter and less than a surface area of the base.

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